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1. Your reference — 100024/WJN

2. Patent application number *(The Patent Office will fill in this part)* — 0025592.7 — 18 OCT 2000

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

   STMicroelectronics Limited
   1000 Aztec West,
   Almondsbury,
   Bristol, BS32 4SQ

   Patents ADP number *(if you know it)* — 74627001

   If the applicant is a corporate body, give the country/state of its incorporation — United Kingdom

4. Title of the invention — INTERFACE DEVICE

5. Name of your agent *(if you have one)* — Page White & Farrer

   "Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

   54 Doughty Street
   London WC1N 2LS

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   a) any applicant named in part 3 is not an inventor, or
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12. Name and daytime telephone number of person to contact in the United Kingdom: W J Neobard 020-7831-7929

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INTERFACE DEVICE

The present invention relates to a communication device suitable for debugging a digital processor on a single integrated circuit chip, the chip comprising an on-chip emulation device.

Known techniques for debugging embedded digital processors include the use of on-chip emulation devices whose function is to monitor and control the operation of the digital processor. Such on-chip emulation devices typically have storage capability, and the ability to initiate command and control sequences for the digital processor in response to externally applied signals from a host computer or to detected states of the digital processor.

Communication between the on-chip emulation device (oce) and the host computer is carried out via a link, which is typically a link designed for the particular situation. As a result, signals over the link may be tailored to the particular on-chip emulation device in the interests of efficient debugging.

There is however a problem in that the use of a specialized link dictates a physical link dedicated to the system, and also requires the host computer to be running programs dedicated to the production of signals for the on-chip emulation device of concern.

It is proposed in a copending patent application to provide such a chip with a universal serial bus (usb) port and interface for communication with the on-chip emulator.

It is however desirable to further enhance the communication possibilities to such a chip.

According to a first aspect of the invention there is provided a communication device for a target integrated circuit

chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

Preferably the device further comprises an on-chip memory interface for connection to memory in said device but external to said chip.

Advantageously the device further comprises modem circuitry for connection of a telephone line to said universal serial bus.

In one embodiment the modem circuitry comprises a soft modem running on sad on-chip processing circuitry.

In a second embodiment the said modem circuitry comprises a hard modem.

According to a second embodiment of the invention there is provided the combination of a communication device and a target integrated circuit chip, said target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an

Ethernet port for connection to said off-chip circuitry, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

Preferably the combination further comprises modem circuitry for connection of a telephone line to said processing circuitry of said communication device.

According to a further aspect of the present invention there is provided a method of communicating with a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising:
supplying data from said off-chip circuitry via an Ethernet bus to an Ethernet port of a communication device comprising a further integrated circuit chip having on-chip Ethernet interface circuitry and on-chip processing circuitry;
passing said data as an input said Ethernet interface circuitry;
in said Ethernet interface circuitry, translating said data into a form suitable for said on-chip processing circuitry;
supplying said translated data to said on-chip processing circuitry;
processing said translated data to provide output data;
applying said output data to an on-chip universal serial bus interface, for transfer via a universal serial bus to said on-chip emulator of said target integrated circuit chip.

According to yet another aspect of the invention there is provided a method of debugging a target integrated circuit chip using a host computer device, said target integrated circuit having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor according to a host program and to collect operation data from said digital processor for communicating to said host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising
providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface,
connecting said Ethernet port to said host via an Ethernet link;
connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus;
communicating data between said on-chip emulator and said on-chip processing circuitry;
processing data in said on-chip processing circuitry to provide output data; and
supplying said output data to said host via said Ethernet port.

Preferably the method further comprises loading a program from said host to said on-chip processing circuitry over said Ethernet link.

According to a still further aspect of the invention there is provided a method of debugging a target integrated circuit chip having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor and to collect operation data from said digital processor for communicating to a host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising

providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface,

connecting said Ethernet port to said host;

connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus;

communicating data between said on-chip emulator and said on-chip processing circuitry;

processing said data in said on-chip processing circuitry to provide output data;

supplying said output data to said on-chip emulator circuitry.

Preferably the method comprises running an embedded web-server process on said on-chip processing circuitry.

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 shows a block schematic diagram of an integrated circuit chip incorporating an on-chip emulator, the chip having a single on-chip processor;

Figure 2 shows a block schematic diagram of an integrated circuit chip incorporating an on-chip emulator, the chip having plural on-chip processors; and

Figure 3 shows an embodiment of the combination of the device of Figure 1 with a communication device, in accordance with the present invention

In the various figures, like reference numerals indicate like parts.

Referring first to Figure 1, an embedded system includes an integrated circuit chip 100 which comprises a processor 10 on said chip. As used herein, the term `processor' includes microprocessors and digital signal processors. The processor is connected to other component circuitry of said embedded system in a manner known to those skilled in the art.

At least during debugging of said embedded system, it is advantageous to be able to collect information about the operation of the processor and also to supply control and command information to said processor, both in response to conditions on the processor itself, and also in response to information conveyed from a host computer.

For collecting information about operation of the processor and for controlling the processor the chip 100 includes an "on-chip emulator" which comprises storage and processing circuitry for that purpose. Such an on-chip emulator 20 is shown schematically on Figure 1 as having a control path 21 connected to the digital signal processor 10 and having an information-collecting path 22 from the digital signal processor 10.

Typically the on-chip emulator 20 has associated JTAG circuitry 30 connected to it, as known to those skilled in the art.

The chip further comprises a USB interface circuit 40. The USB interface 40 has a first port 41 connected to the on-chip emulator 20, a second port 42 connected on-chip to a USB port 50 via a universal serial bus 51. The USB interface circuitry also has a further port 42 connected to the JTAG circuitry 30 which in turn has an on-chip connection 31 to a JTAG port 60.

A universal serial bus is, in use, connected to the USB port 50. the universal serial bus 52 connects at its other end to a host device, typically a debugging computer having a USB port.

Debugging may take place using the host device; however by virtue of the USB connection, it may be possible to debug from a more remote location, as will be later described herein.

Referring now to Figure 2, a second integrated circuit chip 200 comprises plural, here 3, embedded digital signal processors 110, each having a respective associated on-chip emulator 120 connected to it via a respective control path 121 and information collecting path 122. Each on-chip emulator 120 is connected to respective USB interface circuitry 140 and each USB interface circuitry 140 has a USB input port 142 to which is connected an on-chip universal serial bus 151 which connects to an on-chip USB hub 170. JTAG circuitry as shown in Figure 1 may also be provided but is here emitted for the sake of clarity.

The USB hub 170 has an input for a universal serial bus 152, whereby debugging occurs.

The non-proprietary buses provide the ability to download programs and monitor and control the processor (so-called "peek" and "poke") in combination with a remote or host system. The bus also allows a general bi-directional communication path between the host and target system.

Moreover, by use of the on-chip emulator and the bus there is provided a mechanism through which any processor or peripheral on-chip can remotely access "virtual" devices by means of a proxy process on the host. As an example, a program running on a processor on a chip is able to execute a "socket call" which packages the parameters of the call into a packet. The packet is then sent back over the bus to the host or to an intermediate device which then unwraps the parameters and makes the real "socket call". Such a technique can be used for any software function call.

The use of the non-proprietary bus also enables a route for a host program to configure and control silicon components on a highly integrated device. It enables programming of any on-chip EEPROM and for production programming diagnostics.

During the debugging phase the non-proprietary bus enables coherent control and graphical representation and behaviour of systems on silicon with one or more processors.

Connection to the JTAG circuitry allows for JTAG functions to be executed through the USB port although it should be borne in mind that a JTAG port would still be needed to allow connection to other devices. It will be appreciated by those skilled in the art that whereas JTAG functions normally require a special adapter card this would not be the case using embodiments of the present invention.

Use of the non-proprietary bus allows the multiplexing together of the above-described functions using the bus. A hub would be needed on-chip to enable multiplexing at hardware level. Such a connection is advantageously realized using USB in the 12 Mb/s incarnation since this is in line with Ethernet.

In the state of the art, Ethernet chips are conventionally added at board level. Alternatively real-time hardware emulators are used which provide only limited functionality.

Using chips having USB ports the need for a hardware emulator in the host ceases. Typically, the host may implement a simple proxy server to manage a USB port on the host and which deals with the data from components and functions in the target

device. When a program running on the host needs to communicate to a device or service within the target system, that host program communicates to the proxy server which in turn connects it to the required part of the target. Services include program load and debug, configuration, visualisation, EEPROM programming, running diagnostics, implementation of virtual devices that can be accessed from any CPU within a multiprocessor, or multi CPU systems on silicon device. The embodiment is also capable of Internet access by a simple remote procedure call which requires only a small memory resource on the target which is communicated from the target to the proxy server on the host to convert the remote procedure call into a real socket call. It is envisaged to use a "plug-and-play" set-up for the USB driver.

Referring to figure 3 an embodiment of the present invention will now be described.

A target chip 100, as described with respect to figure 1, is connected via a communication device 700 to a host computer system 800. The communication device 700 has an Ethernet port 750, a universal serial bus port 710 and an integrated circuit chip 701 having on-chip processing circuitry 720, on-chip memory circuitry 721, an on-chip Ethernet interface 740 and an on-chip universal serial bus interface 730. The on-chip Ethernet interface is connected to said Ethernet port via wiring 741, and the universal serial bus interface is connected to the universal serial bus port via wiring 731.The Ethernet port 750 connects to the host via a direct link 751. The on-chip memory circuitry 721 may comprise flash-memory.

Connections on chip link the interfaces to the processing circuitry so that data incoming on the link 751 are translated from the Ethernet protocol to the form chosen for the processing

circuitry 720. Any data to be sent to the target device is output by the processing circuitry 720 to the universal serial bus interface and there translated to the universal serial bus protocol and transferred via the universal serial bus 52 to the target.

In use the on-chip processing circuitry 720 operates using embedded web server processes and the communication device forms an intelligent networked device. The consequence is that it is possible to move certain selected processes from the host onto the on-chip processing circuitry 720. Typically processes suitable for implementation on the on-chip processing circuitry include those that need frequent interaction with the target. Examples of these are filtering debug events, and executing large numbers of detailed configuration scripts. Other processes which could usefully be moved to the circuitry 720 are those which need time-critical interaction with the target where other conditions could prevent the host from such interactions.

Continued reference to Figure 3 shows that the communication device 700 has a further port 760, this being for connection to a telephone line 761. To provide data of the right form for such signalling, the processing circuitry may form a soft modem or alternatively an on-chip hard modem may be provided, as known to those skilled in the art.

Use of the telephone line port enables Internet connection if so required, given the existence of suitable software in the communications device. Alternatively, users can connect their target systems for remote evaluation by, for example, the manufacturer. Yet another alternative is to provide the facility to upgrade or otherwise modify the contents of stored information in the target.

CLAIMS:

1. A communication device for a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

2. The device of claim 1 further comprising an on-chip memory interface for connection to memory in said device but external to said chip.

3. The device of claim 1 further comprising modem circuitry for connection of a telephone line to said universal serial bus.

4. The device of claim 3 wherein said modem circuitry comprises a soft modem.

5. The device of claim 3 wherein said modem circuitry comprises a hard modem.

6 The combination of a communication device and a target integrated circuit chip, said target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry,

and a target on-chip universal serial bus interface connected to said on-chip emulator, the communication device comprising an Ethernet port for connection to said off-chip circuitry, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface, said on-chip Ethernet interface being connected to said Ethernet port, the said interfaces being connected to said processing circuitry for translating between Ethernet protocol data on an Ethernet bus connected to said Ethernet port and universal serial bus data for said target on-chip universal serial bus interface.

7. The combination of claim 6 further comprising modem circuitry for connection of a telephone line to said processing circuitry of said communication device.

8. A method of communicating with a target integrated circuit chip having a digital processor, an on-chip emulator for controlling said digital processor and for collecting operation data from said digital processor for communicating to off-chip circuitry, and a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising:

supplying data from said off-chip circuitry via an Ethernet bus to an Ethernet port of a communication device comprising a further integrated circuit chip having on-chip Ethernet interface circuitry and on-chip processing circuitry;

passing said data as an input said Ethernet interface circuitry;

in said Ethernet interface circuitry, translating said data into a form suitable for said on-chip processing circuitry;

supplying said translated data to said on-chip processing circuitry;

processing said translated data to provide output data;

applying said output data to an on-chip universal serial bus interface, for transfer via a universal serial bus to said on-chip emulator of said target integrated circuit chip.

9. A method of debugging a target integrated circuit chip using a host computer device, said target integrated circuit having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor according to a host program and to collect operation data from said digital processor for communicating to said host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising

providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface,

connecting said Ethernet port to said host via an Ethernet link;

connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus;

communicating data between said on-chip emulator and said on-chip processing circuitry;

processing data in said on-chip processing circuitry to provide output data; and

supplying said output data to said host via said Ethernet port.

10. The method of claim 9 and further comprising loading a program from said host to said on-chip processing circuitry over said Ethernet link.

11. A method of debugging a target integrated circuit chip having a digital processor and an on-chip emulator wherein said on-chip emulator is operable to control said digital processor and to collect operation data from said digital processor for

communicating to a host, said chip comprising a target on-chip universal serial bus interface connected to said on-chip emulator, the method comprising

providing a communication device comprising an Ethernet port, a universal serial bus port and a further integrated circuit chip having on-chip processing circuitry, on-chip memory circuitry, an on-chip Ethernet interface and an on-chip universal serial bus interface,

connecting said Ethernet port to said host;

connecting said communication device to said target on-chip universal serial bus interface via a universal serial bus;

communicating data between said on-chip emulator and said on-chip processing circuitry;

processing said data in said on-chip processing circuitry to provide output data;

supplying said output data to said on-chip emulator circuitry.

12. The method of any of claims 9 - 11 comprising running an embedded web-server process on said on-chip processing circuitry.

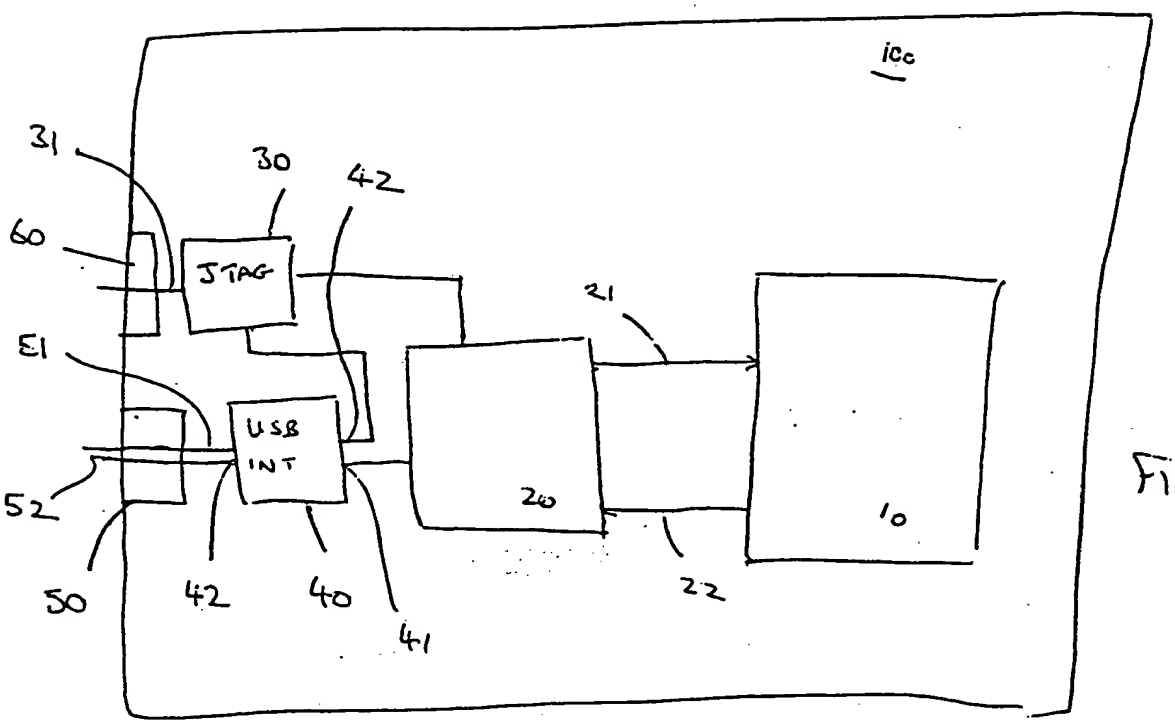
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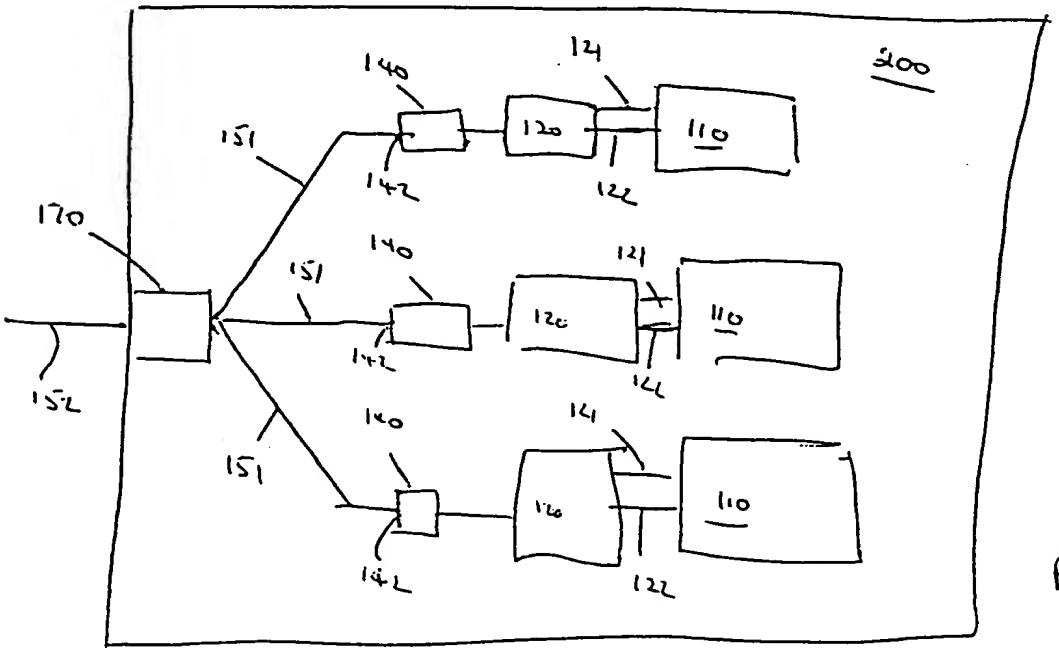
FIG 1


200
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170
140
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124
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FIG 2

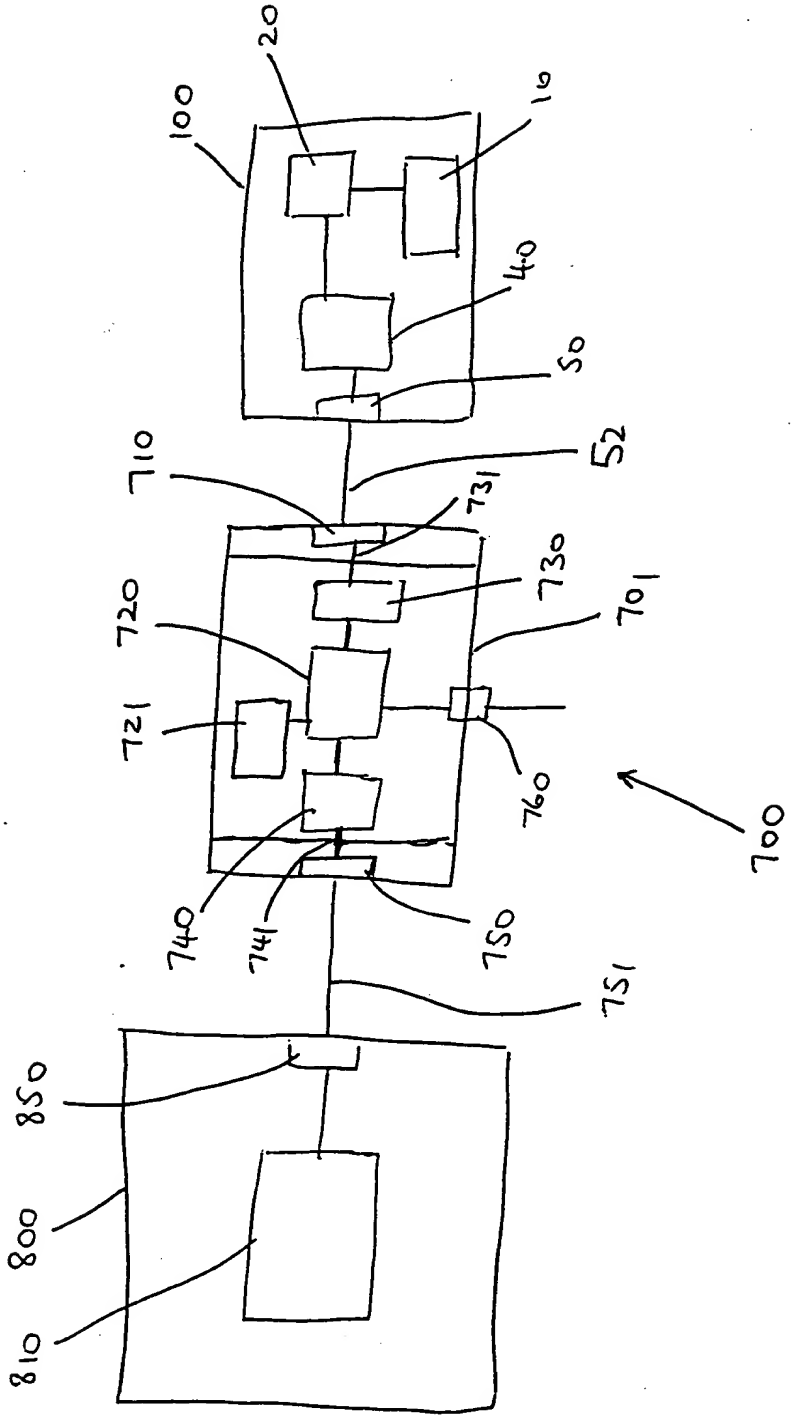
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FIG 3